Slides 1-10
Industry Buzz

Slides 11-59
SFI-5: Technology Overview and
Test Considerations eSeminar

Agilent Technologies

# THE 40G INDUSTRY BUZZ

**April 2, 2002**

***presented by:***

**Larry DesJardin**

# THE 40G Industry Buzz


- Optical Fiber Conference 2002
  @ Anaheim, California
  - 40G Executive Roundtable
  - 40G Announcements
  - Agilent 40G Demonstrations



Agilent Technologies

## 40G Executive Roundtable, sponsored by Agilent Technologies

- Moderated by Peter Heywood, Light Reading & Conard Holton, WDM Solutions
- Attended by 40G executives from across North America, Europe, and Asia.
- Panel of three Agilent 40G executives in each roundtable.

## Economics

- Cost/Bit will determine 40G success, not capacity
- Higher speed has led to lower cost/bit *but...*
- 40G faces additional challenges that may determine when and where it meets cost goals.

# 40G Executive Roundtable

## 40G, What, Where, & When?

- **What first? Executive Vote:**
  - 1st: Short Reach (Switches, Routers)
  - 2nd: Metro DWDM
  - 3rd: Long Haul DWDM

- **Which geographies? Executive Vote:**
  - North America first
  - Followed by Europe
  - Asia 3rd, L-band in Japan

- **When? Executive vote:**
  - First real deployments: 2004
  - First large volumes: 2005




Agilent Technologies

# 40G Executive Roundtable

## Winning Standards

- SFI-5..... Definitely!
- VSR: 1550 serial first, 1310 later..Yes!
  850nm 12x3.3G in 2003.....Yes!
  CWDM.....perhaps
- OC-768, STM-256....of course!
- G.709 (OTN)...”we’d rather not say, we are doing *something*, but we can’t discuss it.”

## 40G Executive Roundtable Wrap-up

- 40G *will* happen (100% vote!)
- Economics will determine where, when
- Short reach applications first large volumes
- Standards play a big role: SFI-5, VSR, OTN,...
- Economics, Industry health will modulate 40G ramp-up
- Great discussions!

# OFC 40G Product Announcements

## 40G Systems

- Lucent Unite (Switch) and Xtreme (DWDM system)

## 40G Components

- Agere, AMCC, Core Optics, GigaTera, Infineon, Inphi, JDSU, Nortel, NEL, Quake, ...and many more!

# Agilent 40G Product Demonstrations

## Agilent 40G Demonstrations:

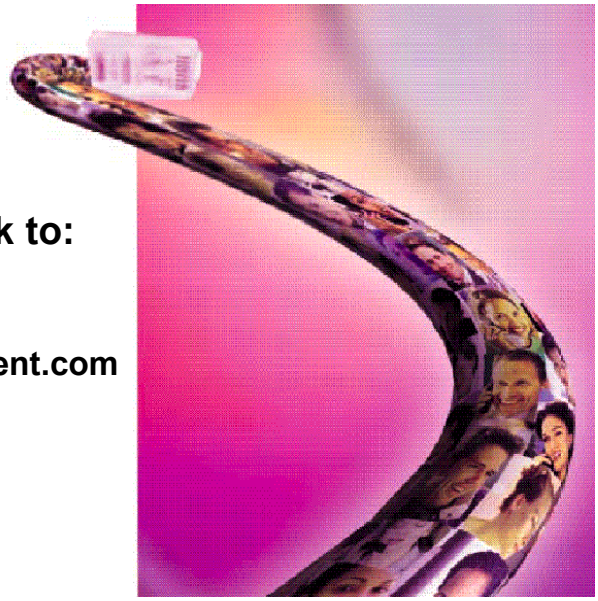
- rAPTor All-Parameter Test
- Optical Dispersion Analyzer
- Precision Wavelength Meter
- >500Ghz Optical Sampling DCA
- Remote Sampling Heads for DCA
- JS-1000 Jitter System
- 43G ParBERT electrical BERT
- 43G Optical BERT system
- ...and more.....!




Agilent Technologies

Agilent Technologies

# THE 40G INDUSTRY BUZZ



Send any feedback to:

larry_desjardin@agilent.com

Agilent Technologies

# SFI-5 Technology Overview and Test Considerations

**April 2, 2002**

***presented by:***

**Anthony Sanders, Infineon**
**Michael Fleischer-Reumann, Agilent**

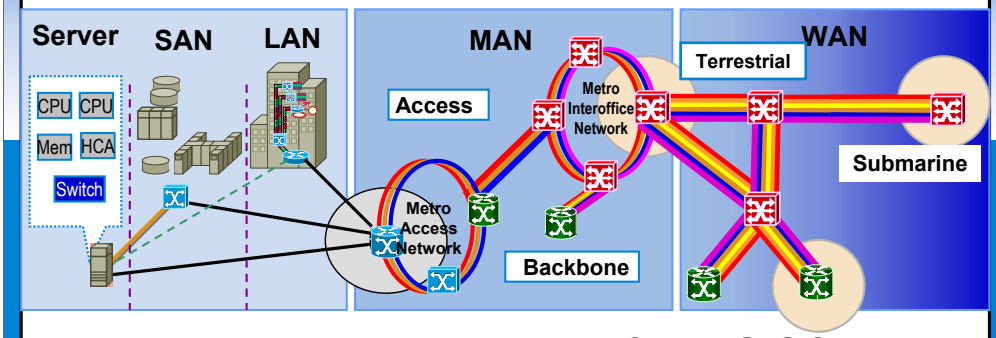
# Agenda

- SFI-5 Technical Overview
  - SFI-5 and line card architecture
  - Synchronous vs. a-synchronous bus
  - Realisation of deskew
  - Clocking concepts
  - Electrical specs
  - Jitter / Wander
- Measurement considerations
  - Necessary test equipment
  - Mux tests
  - DeMux tests

# What is OIF (http://www.oiforum.com)

- Mission: "… foster the development and deployment of interoperable products and services for data switching and routing using optical networking technologies …"
- Physical & Link Layer Work Group of the Technical Committee focus on specific areas where there is a need for Implementation Agreements:
  - VSR-4, VSR-5
  - SFI-4, SPI-4 (SxI-4)
  - SFI-5, SPI-5 (SxI-5)
  - TFI-5
  - ...

# Where in the Net is SFI-5?

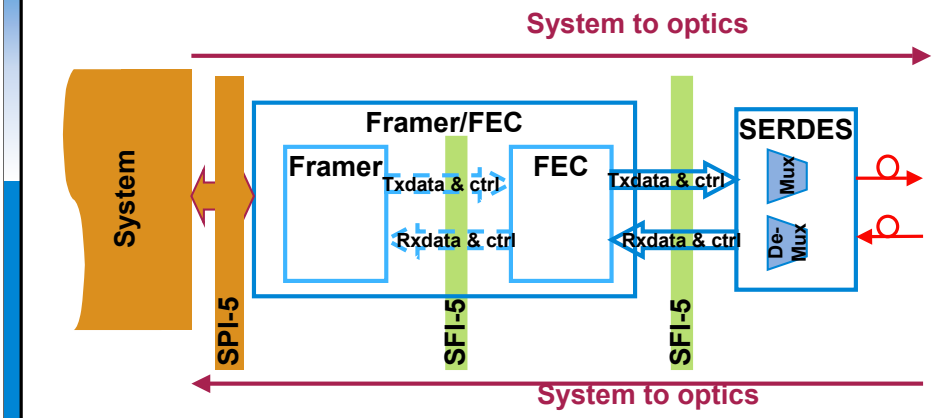



- ADMs, switches and routers for 40G/OC-768 line rates will contain SFI-5 interfaces
- VSR5-links in and between central offices will also have an SFI-5 interface



Agilent Technologies

# SFI-5 architecture block diagram




- Additional Forward Error Correction (FEC) capability may not be integrated into the framer chip; then the SFI-5 appears a 2nd time between Framer and FEC
- The electrical specs on the SPI-5 are identical to the SFI-5, sometimes abbreviated Sxl-5



Agilent Technologies

**SFI stands for: SerDes-Framer-Interface**

**5 stands for the aggregate BW of ~40Gb/s**

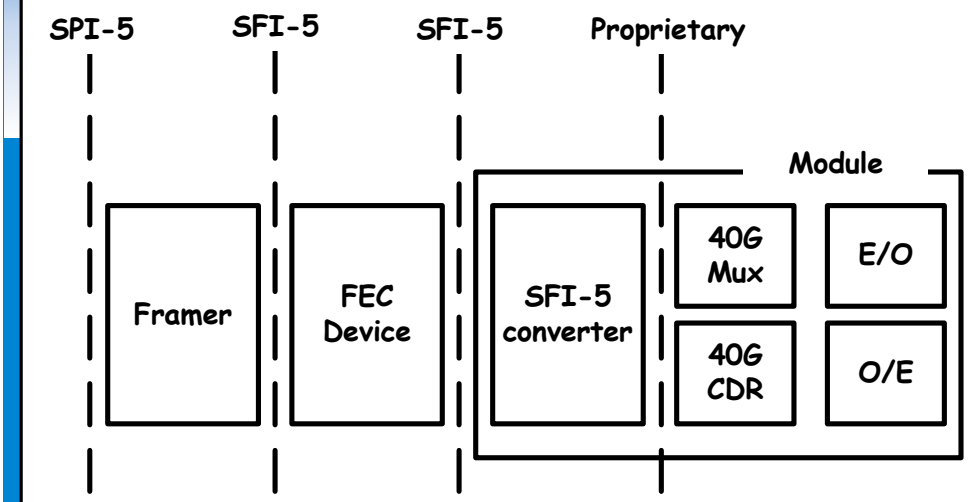
**SFI-5 is a 16 bit-wide parallel data bus running at 2.488-3.125Gb/s data rate resulting in an aggregate BW of 40-50 Gb/s.**

**It has a co-directional clock signal which runs at a quarter rate.**

**Do not mix-up SFI with SPI=System-Packet-Interface**

**SFI-5 does neither specify the architecture of the SerDes circuits themselves nor does it give any specification for the "PHY" e.g. 12x3Gbps, Multi-lambda, 40G Serial.**

# Line Card Substructure



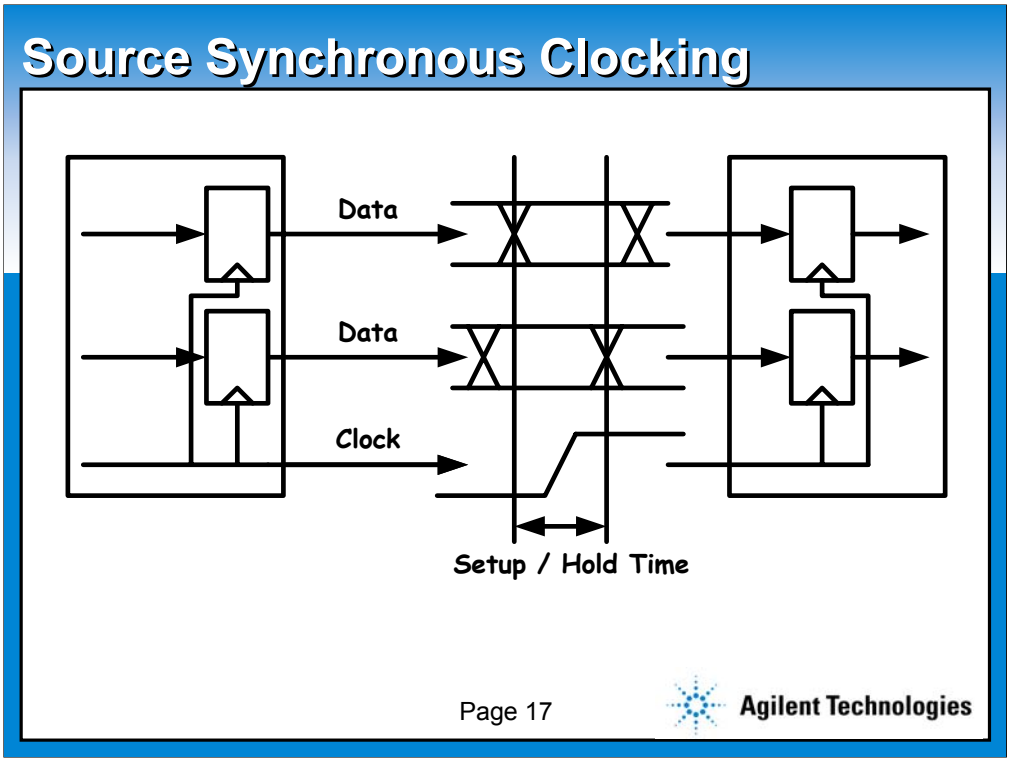



Agilent Technologies

**A typical 40G Line Card solution consists of a Framer / FEC chip set directly on the line card, and a plug-in module solution.**

**The Framer /FEC Asics are ideally developed in a 0.13um CMOS technology with integrated SFI-5 and SPI-5 interfaces.**

**In the module the best technology partition consists of a CMOS solution for the SFI-5 interface, and a SiGe or InP solution for the 40G Serialisation. The interface between the CMOS and Bipolar being optimised for power.**

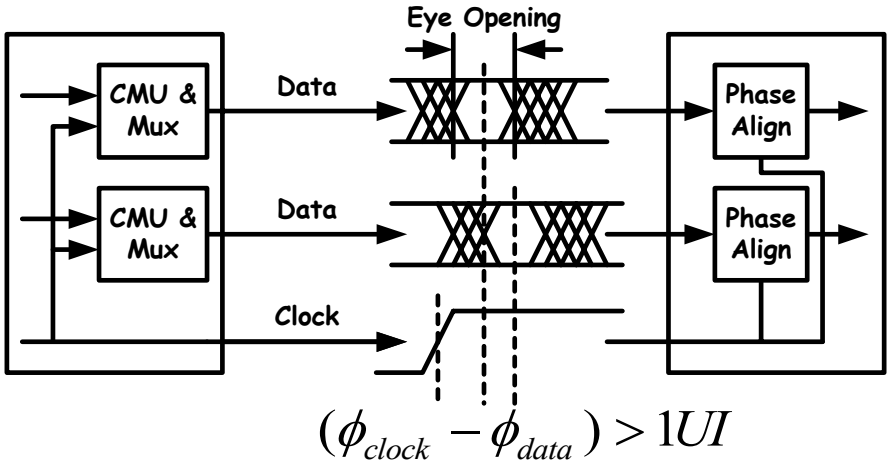



**Traditionally the SerDes Framer interface was Source Synchronous e.g SFI-4.1.**

**This means that the total Skew & Wander between data lines and the clock is limited to one period minus the setup and hold time of the receiver.**

**Given correct design of the interface only a single clock at the receiver is required to sample all of the data line simultaneously.**

## Channel Based




$$(\phi_{clock} - \phi_{data}) > 1UI$$



Agilent Technologies

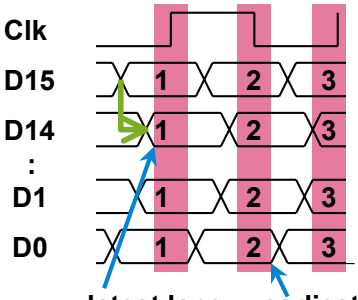
**As the baud rate increases it becomes impossible to control the relationship between the data channel, and a Channel Based interface must be adopted i.e. SFI-5.**

**Here the Skew & Wander between data and clock can exceed a single bit period, and therefore no single clock can sample all data channels simultaneously.**

**A Clock for each channel must be recovered, which tracks the incoming data. This recovery can be achieved by performing a independent phase alignment of the divided clock for each data channel.**

# Synchronous vs. A-synchronous

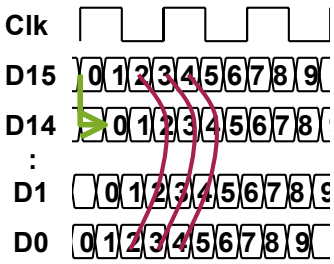
**SFI-4**
**synchronous parallel bus with common data valid time**




**latest lane determines set up time**

**earliest lane determines hold time**

**SFI-5**
**a-synchronous "parallel" bus without common data valid time**

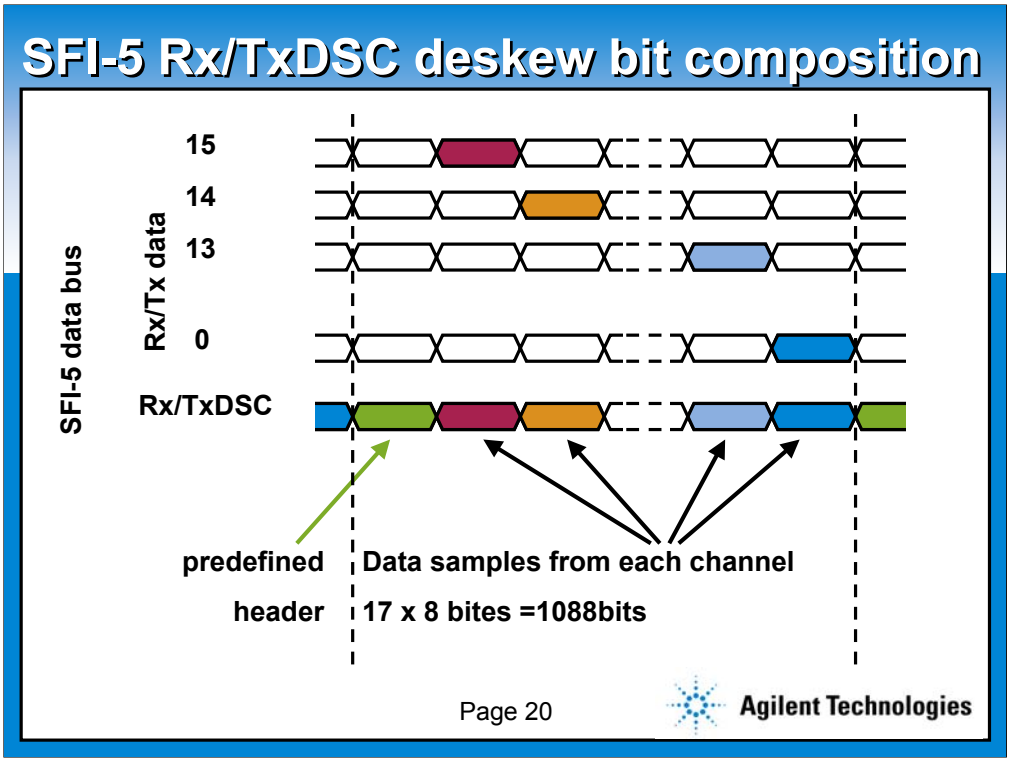



**same absolute delays at 4-fold data rate result in > 1 UI skew!**
**=> no common data valid time**



Agilent Technologies

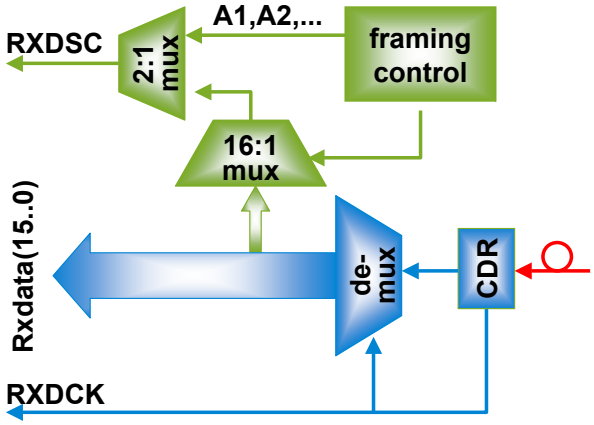
**As each channel can independently wander by more than a single period, the word relationship of the parallel is lost through multiplexing and de-multiplexing.**




**De-skewing is achieved by the 17th bit (TXDSC or RXDSC), which contains data samples from each of the 16 data channels, each 8 bytes long, in a round robin fashion following after an 8 byte header.**

# Deserializer / demux block diagram

- Main functionality is the demux circuit itself
- SFI-5 circuitry generates 17th RxDSC-bit, consisting of header (A1-A1-A2-A2-EH1- … - EH4) and data samples from D15 to D0





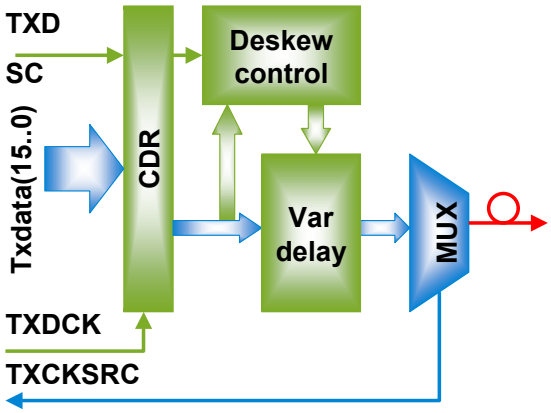

Agilent Technologies

**The DSC channel is easily generated by multiplexing the 16 channels together with the framing information.**

# Serializer (mux) block diagram

- Main functionality lies in the mux itself, which achieves the 40G
- SFI-5 circuitry enables the mux as it deskews the loosely timed input signals

(poorly timed by stimulating IC and further distorted by PC board)

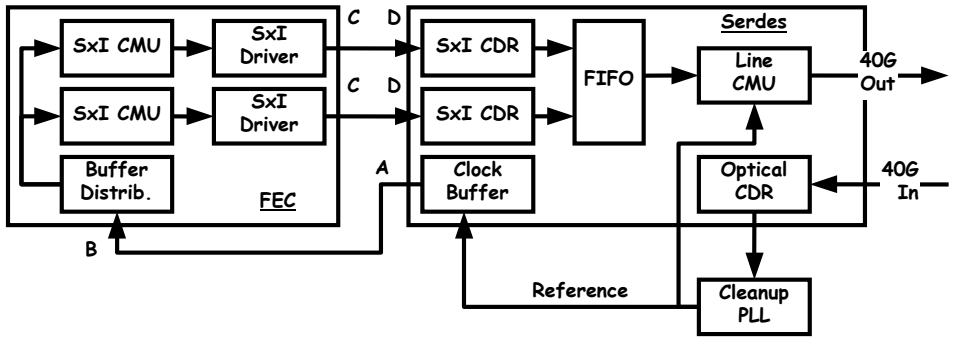





Agilent Technologies

**De-skew is performed by a control block which monitors the DSC channel and controls the delay of each channel.**

# Reverse Clocking Mode






Agilent Technologies

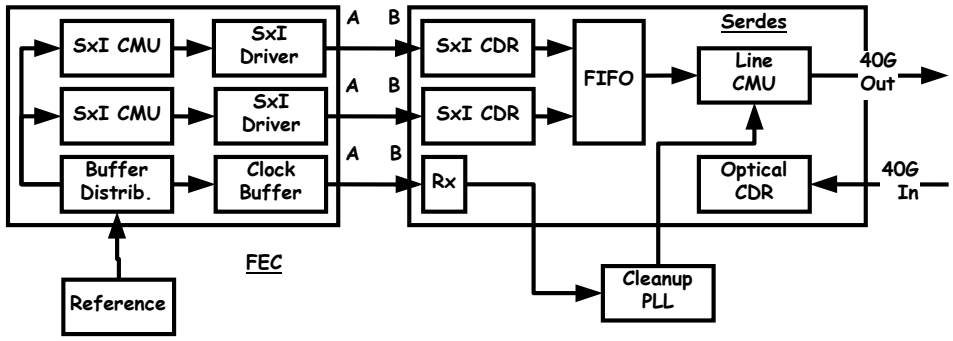
**The jitter present on the SFI-5 signals is a function of the clocking mode of the 40G SerDes.**

**Within 40G there exists two major clocking modes, as shown in the next two foils.**

- **Forward**
- **Reverse**

**The relative amount of jitter present on a signal is represented by “A”, “B”, “C”, or “D”, “A” being the best quality, and “D” being the worst.**

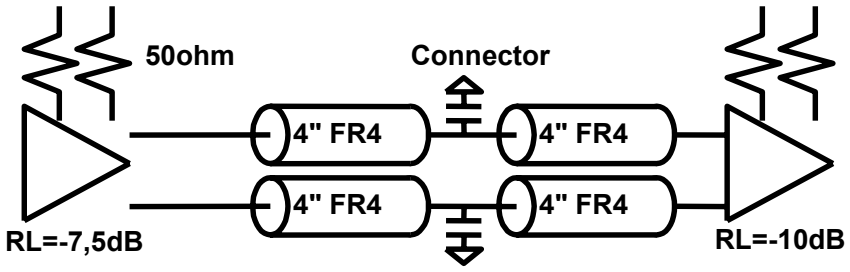
# Forward Clocking Mode






Agilent Technologies

# Channel Model Electrical Description



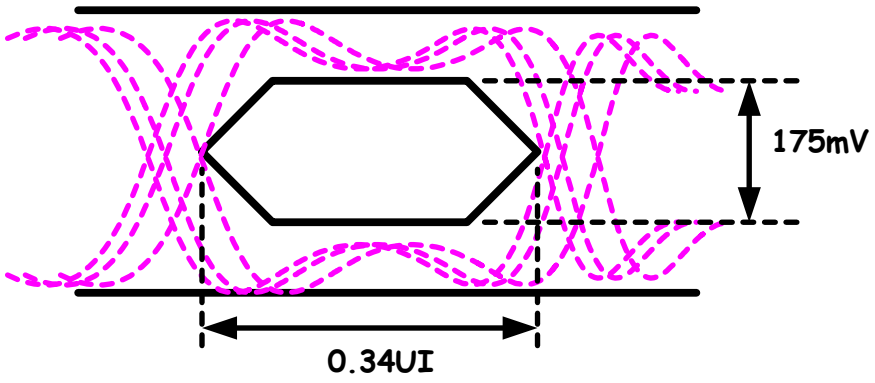

- SFI-5 is a 1v2 DC Differential CML interface
- AC Coupling is optional for chips developed in CMOS technologies >0.13um
- Interface is 50ohm and allows in the jitter and signal budget for 8” of FR4 and one connector



Agilent Technologies

RL = Return Loss

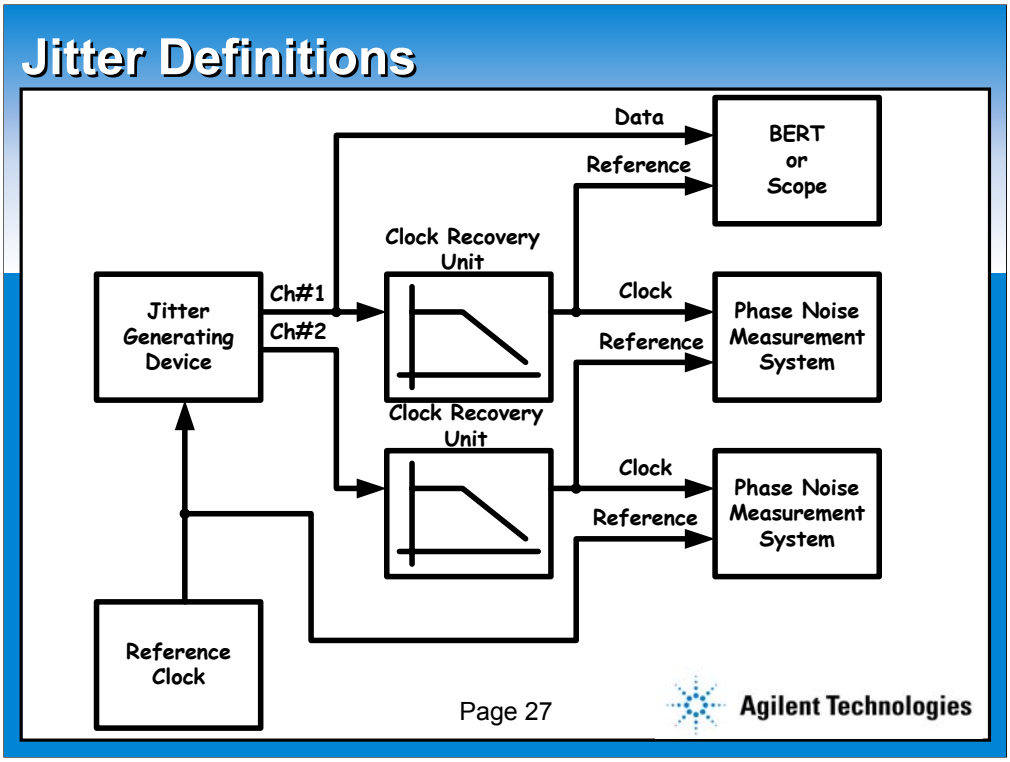
# SFI-5 Data Eye






Agilent Technologies

**SFI-5 defines the electrical signalling for the data as a differential receive data eye, with a given eye opening. When DC coupled the common mode at the transmitter and receiver must in addition lie with defined limits.**




**In exactly the same way that jitter is defined by the ITU, the OIF defined different types of jitter that must be measured and tested for the SFI-5 interface.**

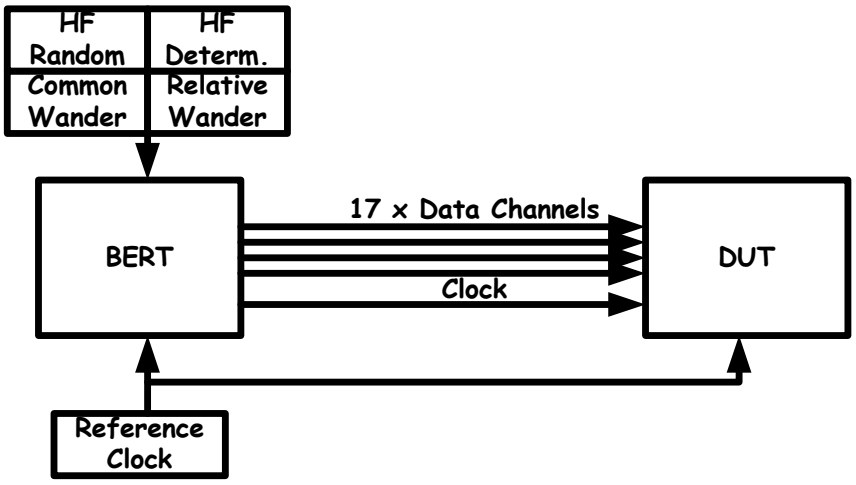
**Common Wander is measured using a Clock Recovery Unit and Phase Measurement System. As shown above the inherent clocking information in Ch#2 is extracted and compared to the reference clock for the device. The amount of common wander on the transmit channel defines the dimensioning of internal FIFO at the receiver.**

**Relative Wander is measured using two Clock Recovery Units. As shown above the extracted clocks from Ch#1 and Ch#2 are compared to one another. The amount of relative wander is important in the design of the de-skew algorithm which can only cancel a maximum amount.**

**HF Jitter is measured using a BERT triggered from a Clock Recovery Unit. As shown above the clock from Ch#1 is extracted and used a trigger for the BERT. HF Jitter defines the amount of non-trackable jitter and effective eye opening at the receiver.**

**The Corner Frequency of the Clock Recovery Units defines the boundary between HF Jitter and Wander and determines the required bandwidth of the clock & data recovery at the receiver.**

# Jitter Tolerance

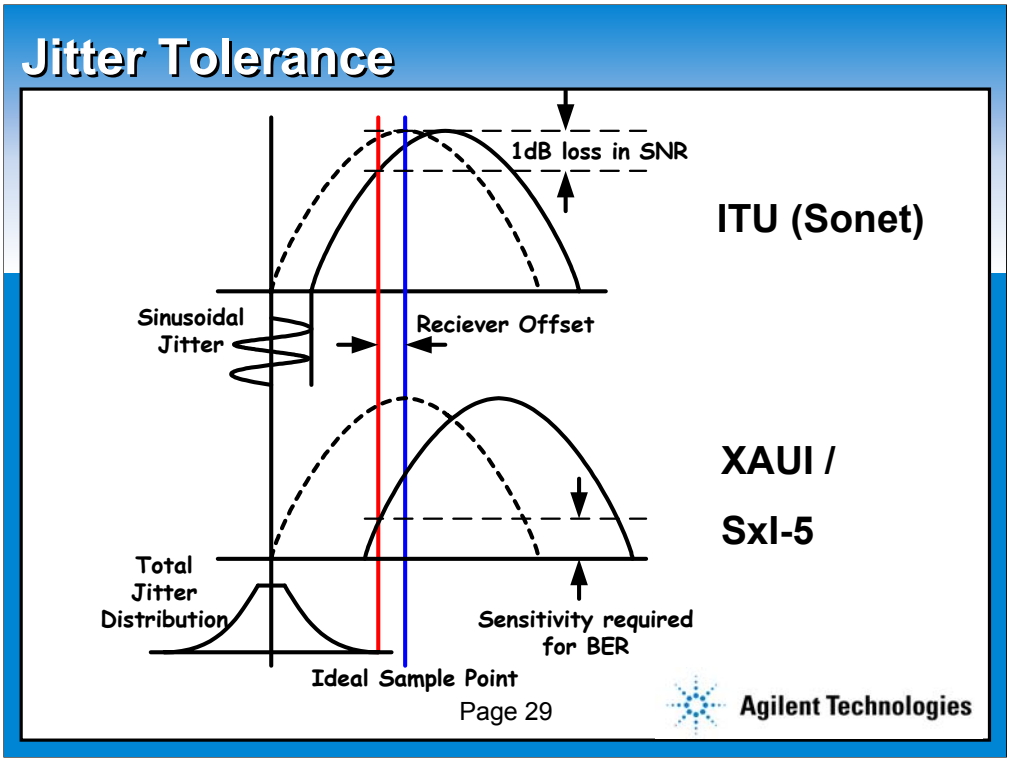





Agilent Technologies

**Jitter tolerance can be considered as being the generation of a test signal with a calibrated amount of jitter, and the measurement of the relative or absolute Bit Error Rate performance of a Device.**

**The calibrated jitter, can be a combination of different types of jitter e.g. HF Bounded Deterministic, HF Random, Common Wander, Relative Wander or simply sinusoidal.**




**ITU defines Jitter Tolerance for OC-192 or OC-768 in terms of a 1dB relative sensitivity loss for a given sinusoidal time jitter.**

**Ethernet and SFI-5 defines Jitter Tolerance in terms of an absolute BER for a given Total Time Jitter, for example for testpoint "D"**

- **0,55UI HF Jitter (Random + Deterministic)**
- **10,65 .. 0,10 UI Common Wander @ 16kHz .. 20MHz**
- **1,30 .. 0,10 UI Relative Wander @ 16kHz .. 20MHz**

**The TOP figure shows an electrical '1', with an applied sinusoidal jitter and it's relative loss of sensitivity at the sampling point of the receiver, due to offset. It can be seen as the amplitude of the sinusoidal jitter is increased, or the offset of the receiver is larger so the loss in SNR of the electrical '1' is increases.**

**The BOTTOM figure shows an electrical '1', with a time distributed jitter. This distributed jitter consists of a bounded deterministic part and a gaussian random part. It can be seen that when the data eye is jittered what the receiver sensitivity must be for a given maximum time deviation. This maximum deviation is defined as the peak to peak of the deterministic jitter plus the RMS of the random jitter multiplied by a factor determined by the required BER.**

# Agenda

- SFI-5 Technical Overview
  - SFI-5 and line card architecture
  - Synchronous vs a-synchronous bus
  - Realisation of deskew
  - Clocking concepts
  - Electrical specs
  - Jitter / Wander
- Measurement considerations
  - Necessary test equipment
  - Mux tests
  - DeMux tests

# List of measurements

| | Measurements | Test Equipment |
|---|---|---|
| Mux | transmit path 2.5G => 40G |   |
| | static skew tolerance / deskew functionality | |
| | parallel jitter tolerance | |
| Demux | receive path 40G => 2.5G | |
| | output waveform | |
| | output skew | |
| | 17th bit data content | |
| | HF Jitter and wander, single channel | 83493A 2.5 Gb/s Single-Mode Clock Recovery Plug-In Module<br>86130 BitAlyzer |
| | relative wander | |



Agilent Technologies

# Test equipment requirements for SFI-5

- **Test equipment must be parallel to stimulate an SFI-5 sink device and to determine e.g. skew of SFI-5 source device such as a de-mux**
- **Not only for "functional" tests but also for acceptance test of parallel and relative wander**
- ***Parallel jitter/wander test sets do not exist today why serial tests sets have to be used (as described before)***

# ParBERT 81250 - a modular system

**adopts to specific needs, e.g. speed, # of channels, and protects investment**

***Front-Ends***

**determine:**

- **type: generator or analyzer**
- **I/O properties**

***Data Modules***

**determine:**

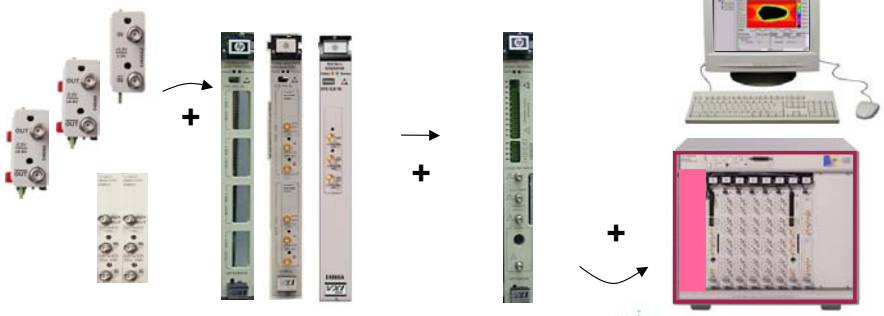
- **signal generation /analysis capabilities**
- **channel speed**

***Clock Modules***

- **determine clock purity**
- **generates the system clock and**
- **distributes clock to Data Modules**

***Mainframe***

- **with different controller options**
- **up to 2 additional expander frames if required**





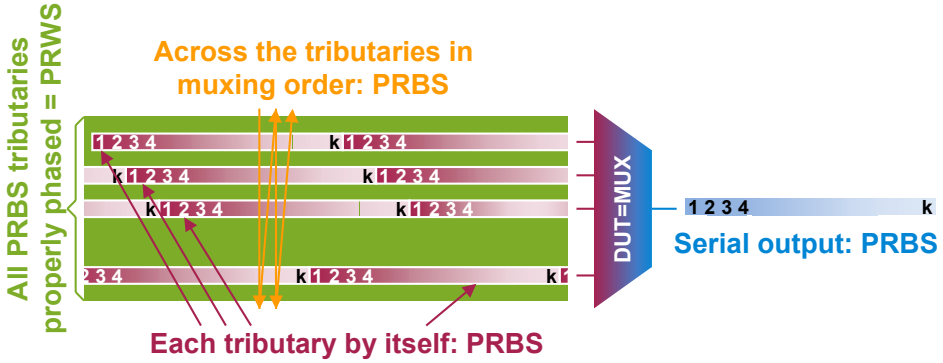
Agilent Technologies

# Mux Test

- PRWS and TxDSC generation
- Test set ups of ParBERT
- Nominal functionality, BER < $10^{-12}$
- Check input skew range
- Simulate closed eye mask
- Test input jitter and wander tolerance

# Stimulating the Mux with PRWS

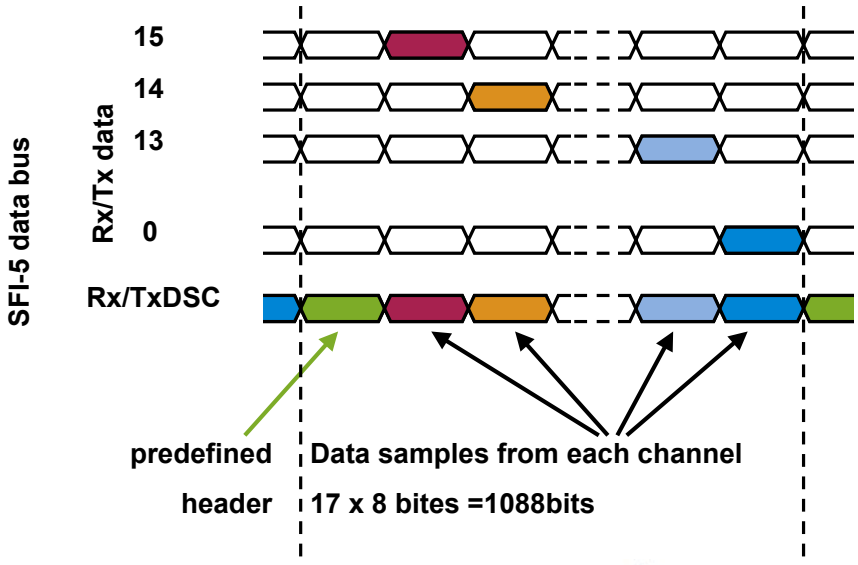
- Desired test pattern on serial side: PRBS of a certain polynomial!
- How must the mux be stimulated to achieve this?
- PRBS sequences on each data line, properly phased: PRWS!






Agilent Technologies

# SFI5 Rx/TxDSC deskew bit composition

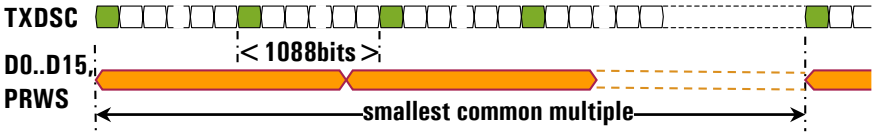





Agilent Technologies

# ParBERT: well suited for parallel bus

- Ports of different nature (data vs clock / NRZ vs RZ)
- With different data rate (2.5Gb/s and 625MHz)
- SFI5 data segment 17 bits wide
  - PRWS $2^7$-1 … $2^{31}$-1 on data0…15
  - Tx/RxDSC with A1-A1-A2-A2-EH1…EH4 header and 8 sample bites of each data channel

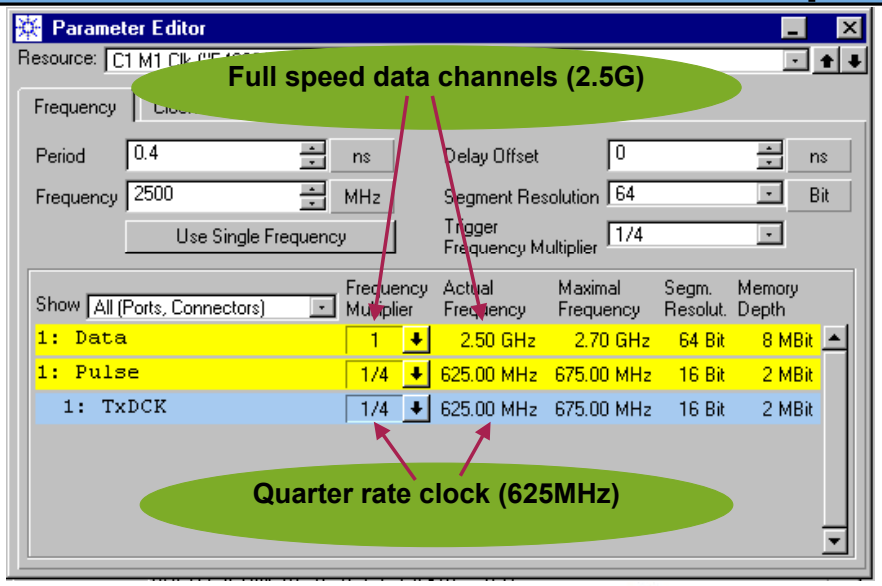



  - for 2.7G modules: memory based $2^7$-1, $2^{11}$-1



Agilent Technologies

# ParBERT GUI: different data rates /port

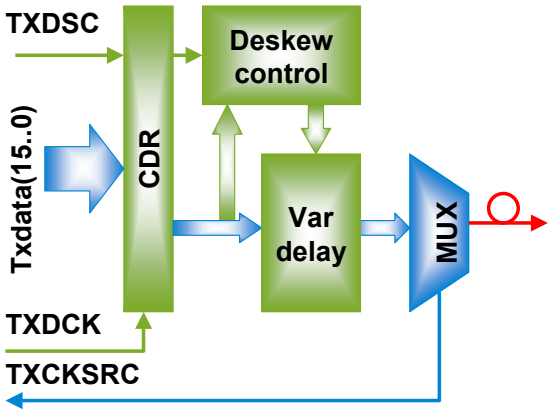





Agilent Technologies

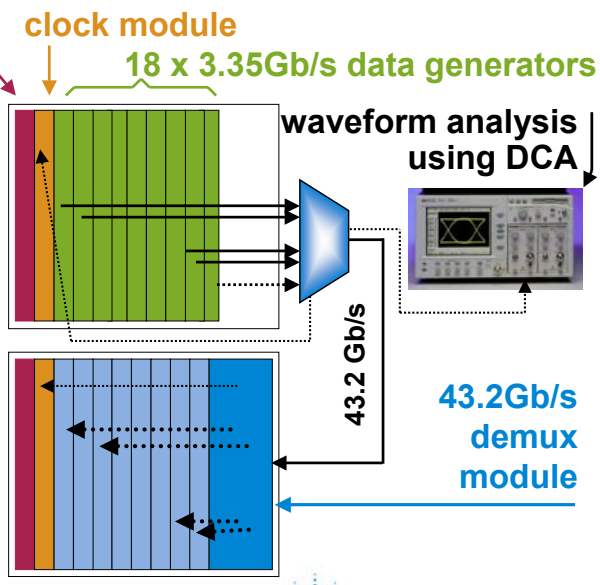
# Serializer (Mux) block diagram

- Test primary mux functionality in terms of
  - BER
  - jitter
  - eye opening
- Test the SFI-5 interface for
  - sensitivity
  - deskew range
  - jitter/wander tolerance



# Test set up for mux

- 18 x 3.35Gb/s Generators for tributaries clock and TxDSC
- 43.2Gb/s Error Detector Bundle consisting of 1:16 demux-module and 16 embedded 3.35Gb/s analyzers





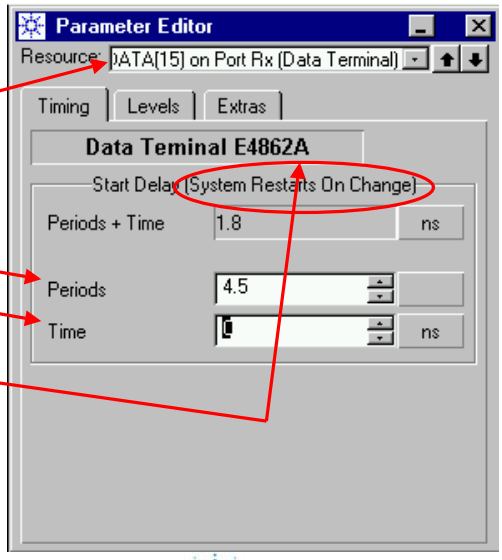

Agilent Technologies

# Check input skew range

- Vary the delay of any desired channel of 17 bit wide data port on the fly (while continuously running)
  - one or more of the 16 data lines Txdata 0 .. 15
  - 17th deskew bit TxDSC
- Check influence of this variation on BER of serial bitstream with 43.2Gbs error detector

# ParBERT GUI individual delay/channel

- Individual skew (delay) of any data bit (Txdata 15) can be entered in UI (Periods) plus Time
- Shown for 2.7G modules (restarts on change) while new 3.35G can do it while running

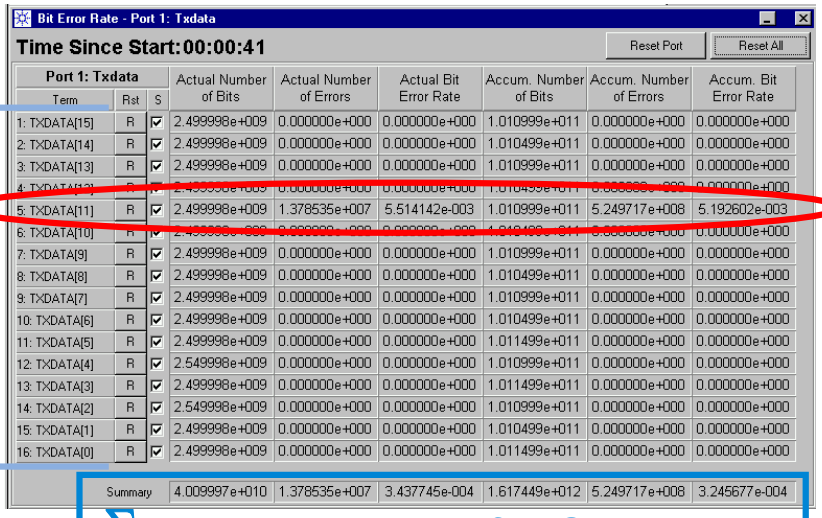





Agilent Technologies

# ParBERT BER GUI result window

Errors of every embedded analyzer



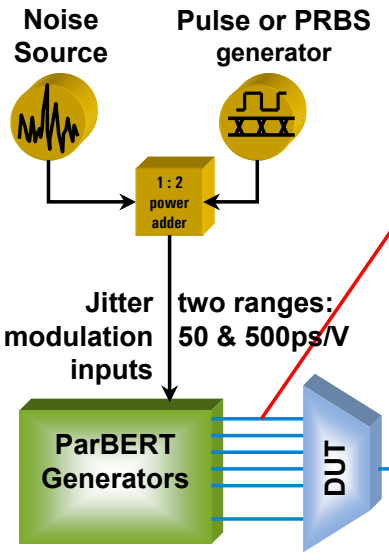

| Port 1: Txdata Term | Rst | S | Actual Number of Bits | Actual Number of Errors | Actual Bit Error Rate | Accum. Number of Bits | Accum. Number of Errors | Accum. Bit Error Rate |
|---|---|---|---|---|---|---|---|---|
| 1: TXDATA[15] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010999e+011 | 0.000000e+000 | 0.000000e+000 |
| 2: TXDATA[14] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010499e+011 | 0.000000e+000 | 0.000000e+000 |
| 3: TXDATA[13] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010999e+011 | 0.000000e+000 | 0.000000e+000 |
| 4: TXDATA[12] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010499e+011 | 0.000000e+000 | 0.000000e+000 |
| 5: TXDATA[11] | R | ☑ | 2.499998e+009 | 1.378535e+007 | 5.514142e-003 | 1.010999e+011 | 5.249717e+008 | 5.192602e-003 |
| 6: TXDATA[10] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010499e+011 | 0.000000e+000 | 0.000000e+000 |
| 7: TXDATA[9] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010999e+011 | 0.000000e+000 | 0.000000e+000 |
| 8: TXDATA[8] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010499e+011 | 0.000000e+000 | 0.000000e+000 |
| 9: TXDATA[7] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010999e+011 | 0.000000e+000 | 0.000000e+000 |
| 10: TXDATA[6] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010499e+011 | 0.000000e+000 | 0.000000e+000 |
| 11: TXDATA[5] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.011499e+011 | 0.000000e+000 | 0.000000e+000 |
| 12: TXDATA[4] | R | ☑ | 2.549998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010999e+011 | 0.000000e+000 | 0.000000e+000 |
| 13: TXDATA[3] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.011499e+011 | 0.000000e+000 | 0.000000e+000 |
| 14: TXDATA[2] | R | ☑ | 2.549998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010999e+011 | 0.000000e+000 | 0.000000e+000 |
| 15: TXDATA[1] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.010499e+011 | 0.000000e+000 | 0.000000e+000 |
| 16: TXDATA[0] | R | ☑ | 2.499998e+009 | 0.000000e+000 | 0.000000e+000 | 1.011499e+011 | 0.000000e+000 | 0.000000e+000 |
| Summary | | | 4.009997e+010 | 1.378535e+007 | 3.437745e-004 | 1.617449e+012 | 5.249717e+008 | 3.245677e-004 |

Σ: Errors and BER of 40G serial side

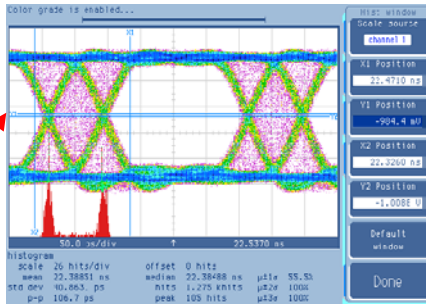


Agilent Technologies

# HF jitter tolerance




Eye opening at receiver



DJ, (RJ) and TJ are user definable through variable amplitude and frequency simple adjustment to different data rates



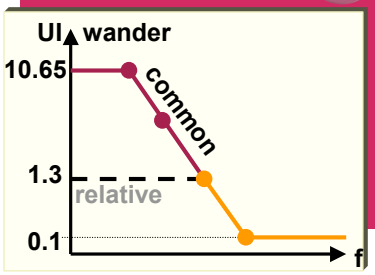
Agilent Technologies

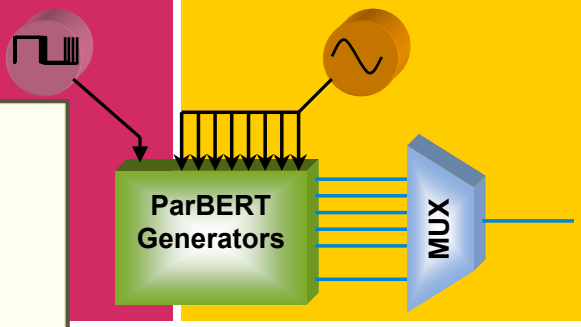
# Common Wander test

Test in two ranges with different setups at discrete frequencies

range 1: >1.3UI, <120kHz
- ParBERT in ext. clock mode
- central clock modulated by external signal generator

range 2: <1.3UI, >120kHz
- ParBERT running at 2.5Gb/s
- modulate generators with 0.8V/UI





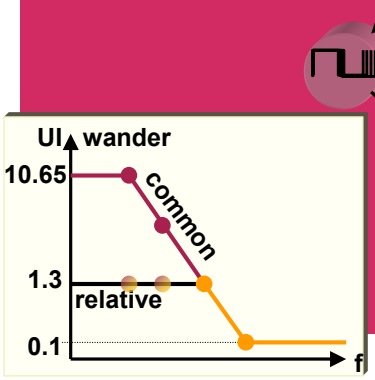

Agilent Technologies

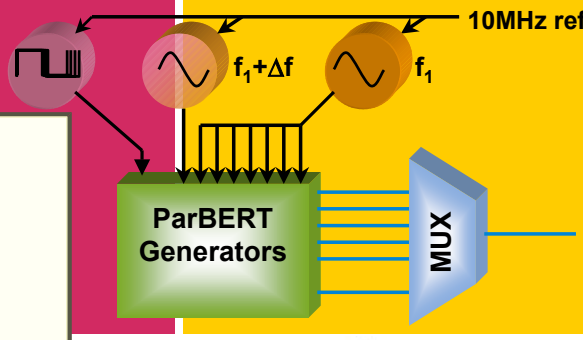
# Common plus relative Wander

Test in two ranges with different setups at discrete frequencies

range 1: >1.3UI, <120kHz
- ParBERT in ext. clock mode
- central clock modulated by external signal generator

range 2: <1.3UI, >120kHz
- ParBERT running at 2.5Gb/s
- modulate generators with slightly different frequencies





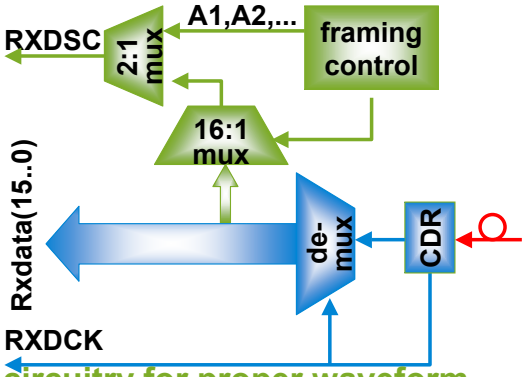

Agilent Technologies

# Demux test

- Test set ups of ParBERT
- Nominal functionality
- Validity of waveform on SFI-5 bus
- Check output skew spec

# Deserializer / demux block diagram

- Test primary De-mux functionality ignoring the RXDSC deskew bit generation circuit
  - BER
  - proper SFI-5 output waveform
  - skew on Rxdata
- Test the SFI-5 specific circuitry for proper waveform and bit content of RxDSC and skew with respect to data bits

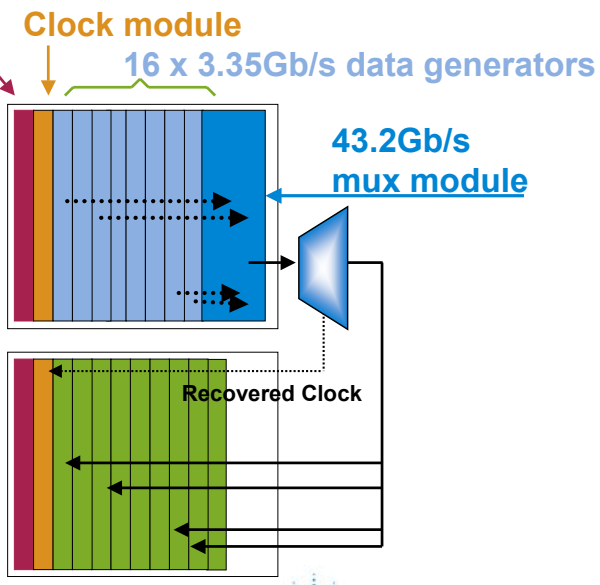





Agilent Technologies

# Test set up for de-mux

- 43.2Gb/s Pattern Generator Bundle consisting of 16 x 3.35Gb/s embedded Generators
- 18 x 3.35Gb/s analyzers for tributaries clock and RxDSC






Agilent Technologies

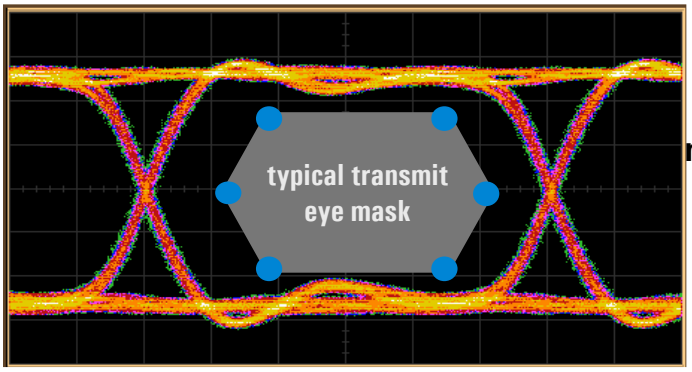
# Nominal functionality

- Stimulate Demux with PRBS (e.g. $2^{31}$-1) on serial side
- Check individual BER of 16 tributary output data lanes Rxdata 0..15

# Validity of waveform on SFI-5 bus

- Verification: fast eye mask verification
- More insight: timing diagrams
- Characterization: eye diagram schmoo

# Verification: fast eye

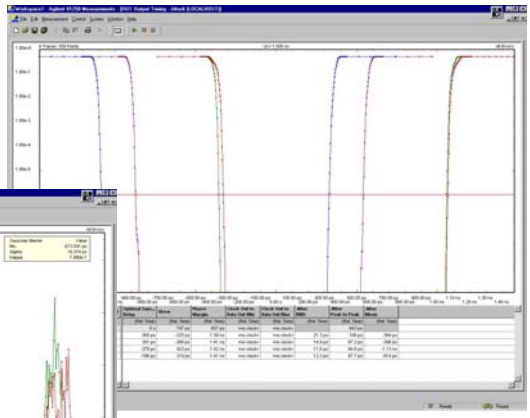


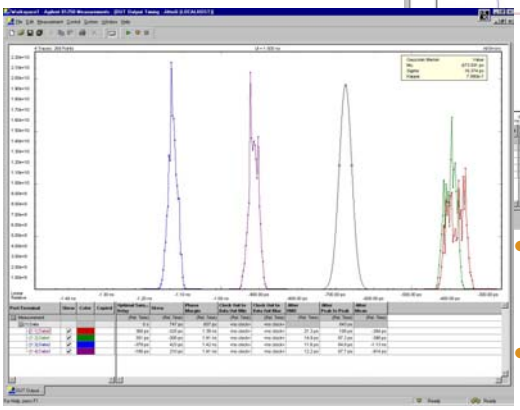

**Pass/ fail measurement for manufacturing**

**Fast eye mask verification**
**check only a few (e.g. 6) points / data lane for BER<$10^{-x}$**

# Insight: output timing measurement

**Horizontal sample point sweep at given voltage threshold**





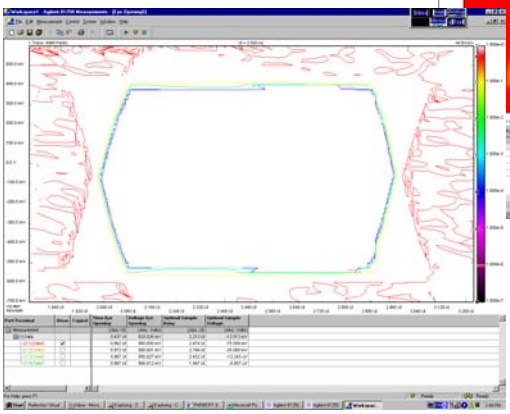
- **Bathtub curve => horizontal opening, skew between channels**
- **Jitter**

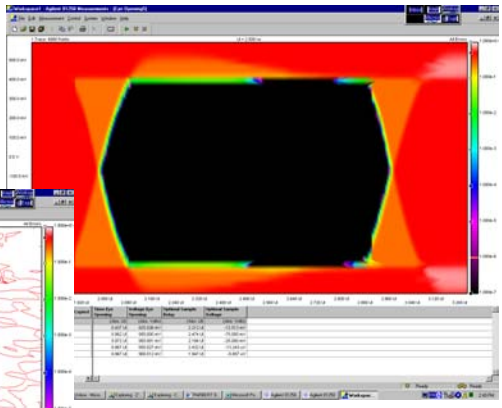


Agilent Technologies

# Characterization: eye diagram / eye-line

**Vertical & horizontal schmoo**





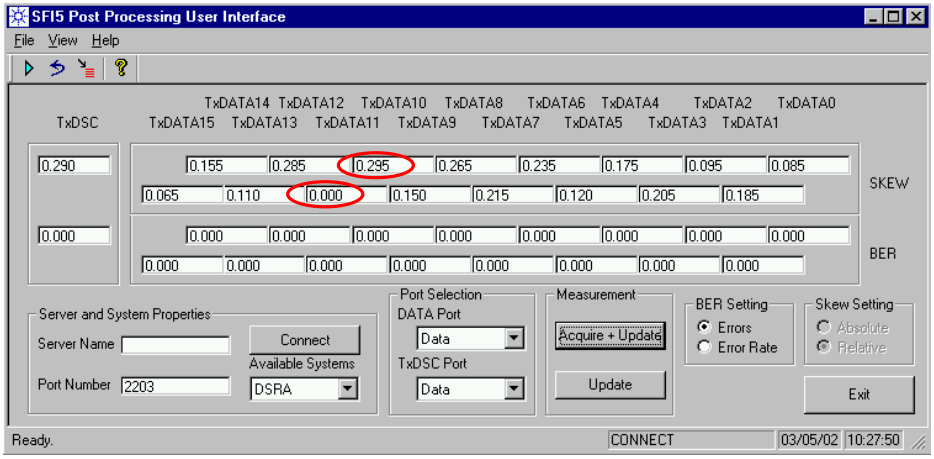


Agilent Technologies

# Check output skew spec

- Stimulate Demux with any PRBS on serial side
- Let ParBERT synchronize, compare (on Rxdata only) and capture Rxdata and RxDSC
- Upload data and run post-processing SW delivering the following results:
  - Bit errors on Rxdata and RxDSC
  - Skew between 17 channels

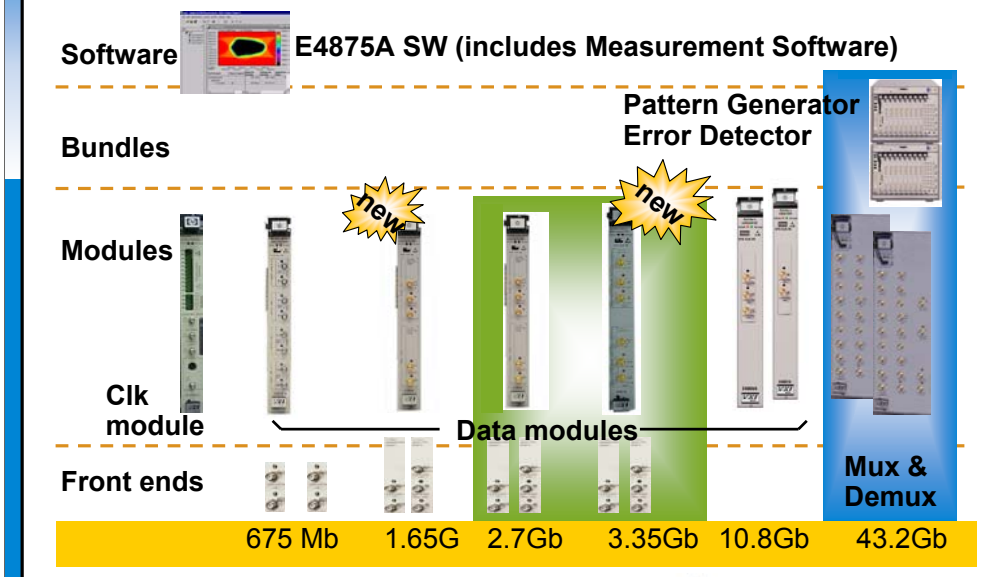
# SFI-5 post-processing SW result display






Agilent Technologies

# ParBERT 81250 - modular system






Agilent Technologies

# Summary

- SFI-5 bus was introduced
  - purpose
  - related measurement issues
- New 3.35G ParBERT modules facilitate SFI-5 testing
- Solutions to some of the SFI-5 measurement tasks were described
- References:

| | |
|---|---|
| *www.oiforum.com* | *OIF* |
| *www.agilent.com/find/parbert* | *ParBERT* |
| *www.agilent.com/find/40Gapps* | *40G App. Central* |

# Test & Measurement Email Updates

**Keep up to date with Agilent's free Test and Measurement Email Updates.**

**As a subscriber, you will receive customized email updates that match your subject and frequency interests.**

**Your updates will include support, products and services, applications, promotions, events and other areas.**

**Subscribe today: www.agilent.com/find/emailupdates**

**Our Privacy Statement at http://www.agilent.com/go/privacy describes our commitment to you regarding your privacy.**

**Please direct any questions about Agilent's privacy program to privacy_advocate@agilent.com.**



Agilent Technologies